

F16. 1

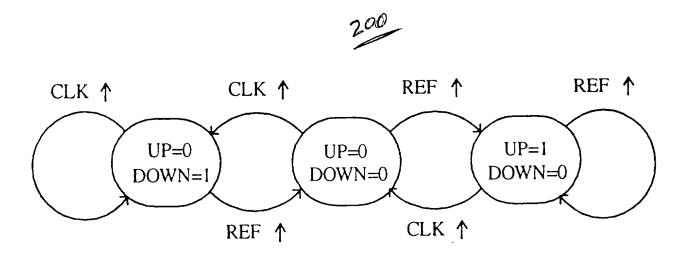
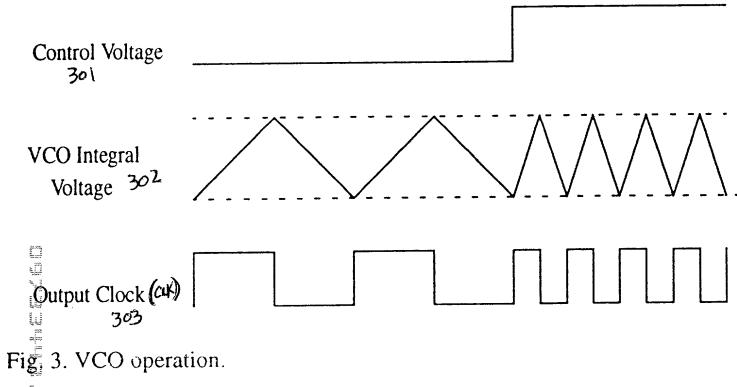
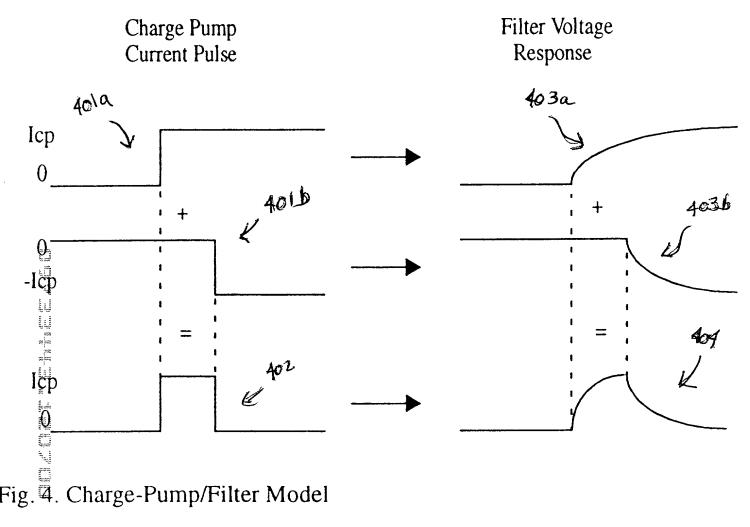


Fig. 2. PFD State Diagram



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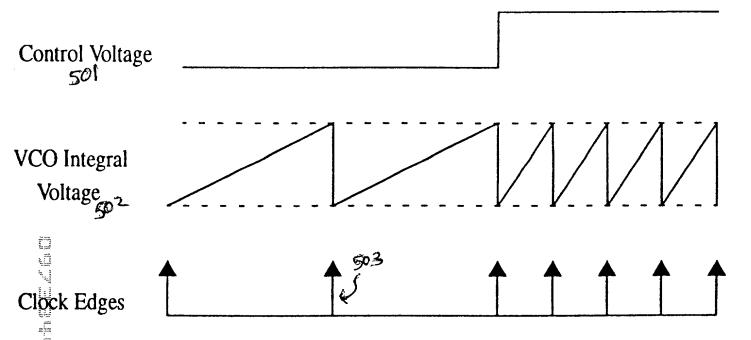


Fig. 5. Mathematical Representation of the VCO

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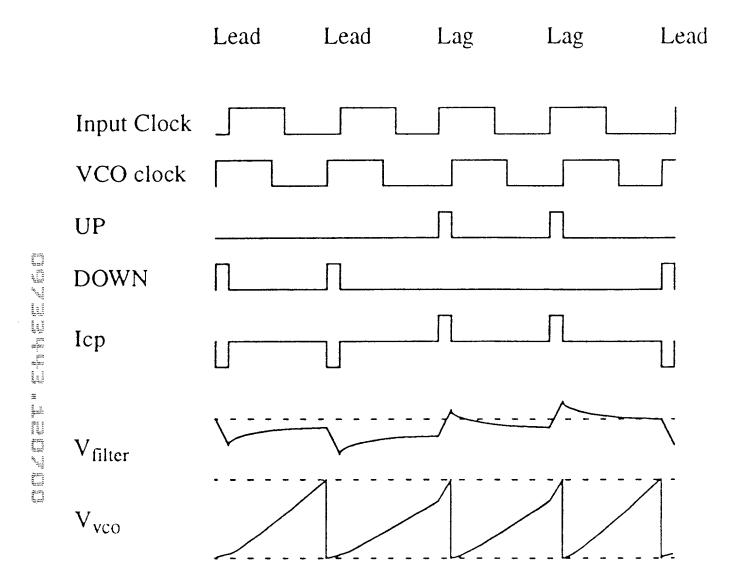


Fig. 6. PLL Operation

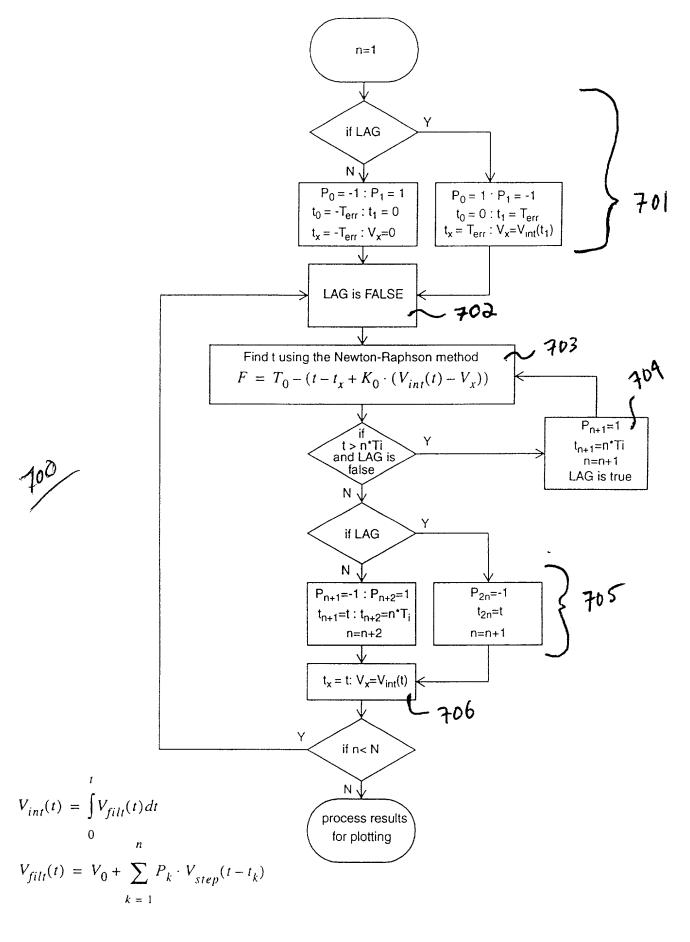
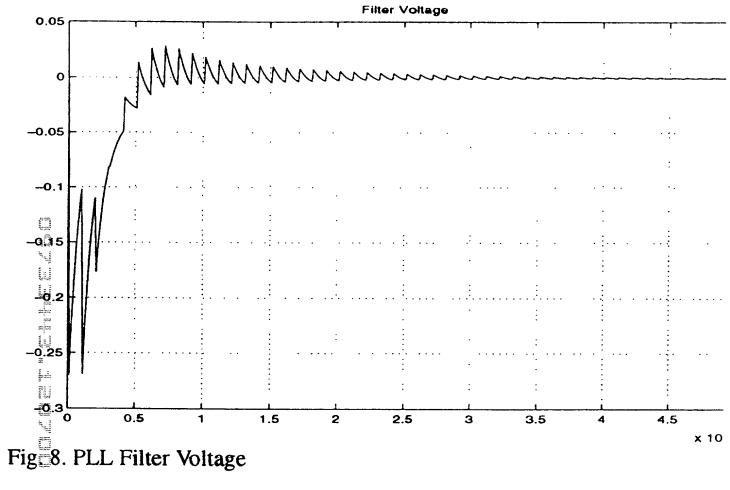
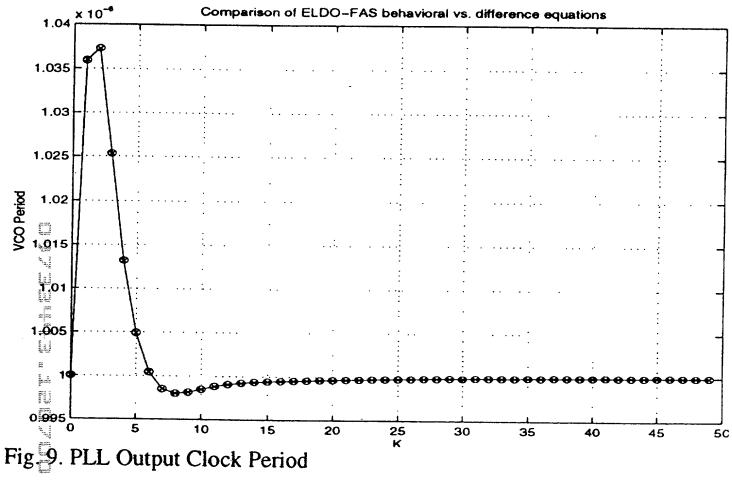
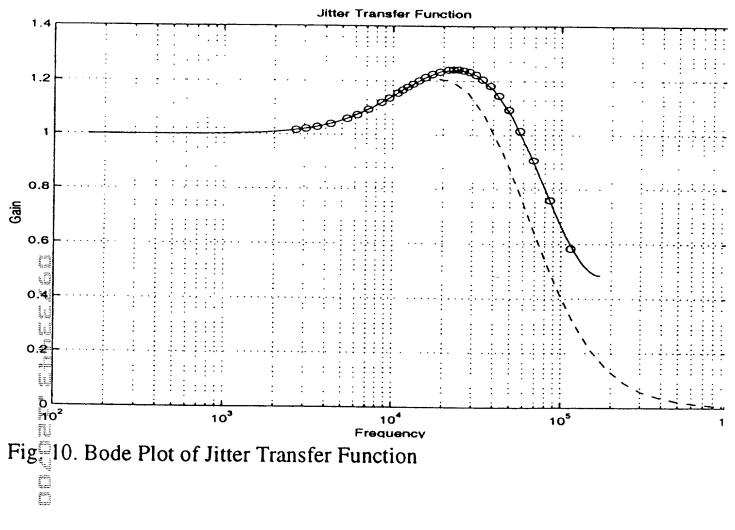
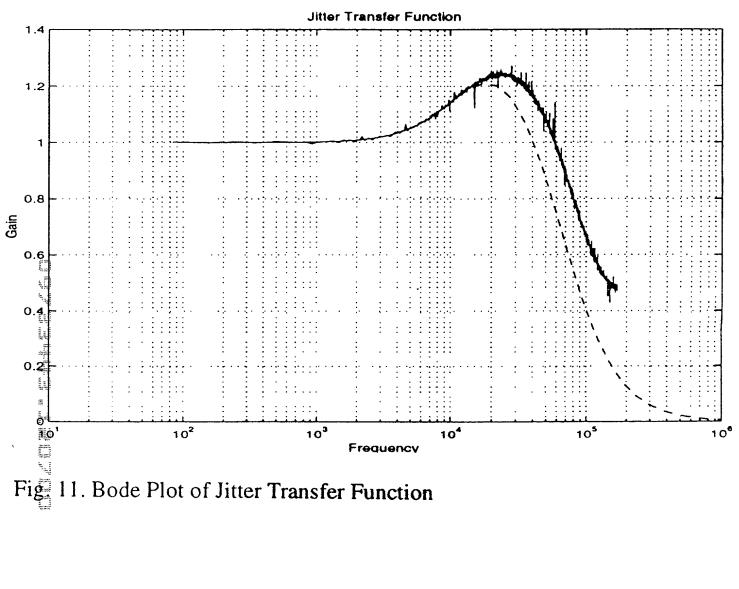


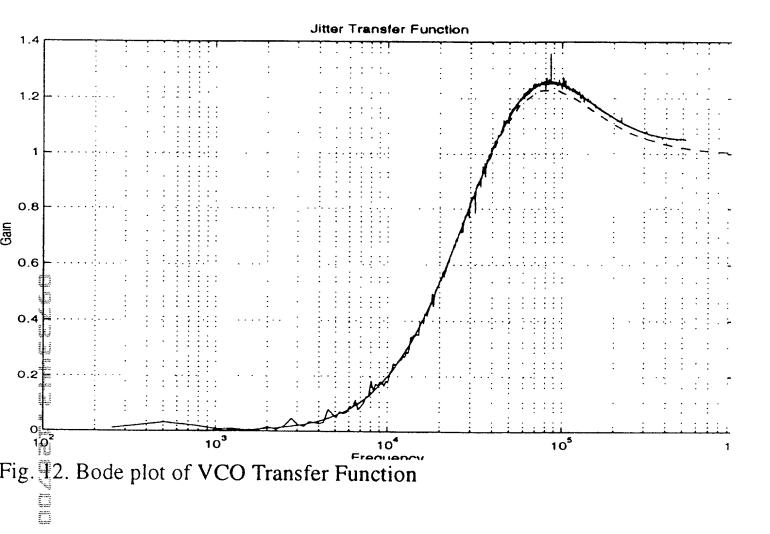
Fig. 7. Model Flowchart











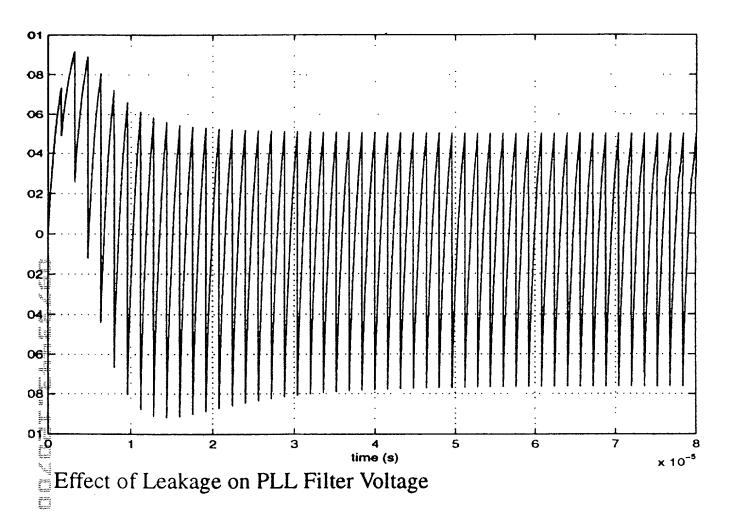


FIGURE 13

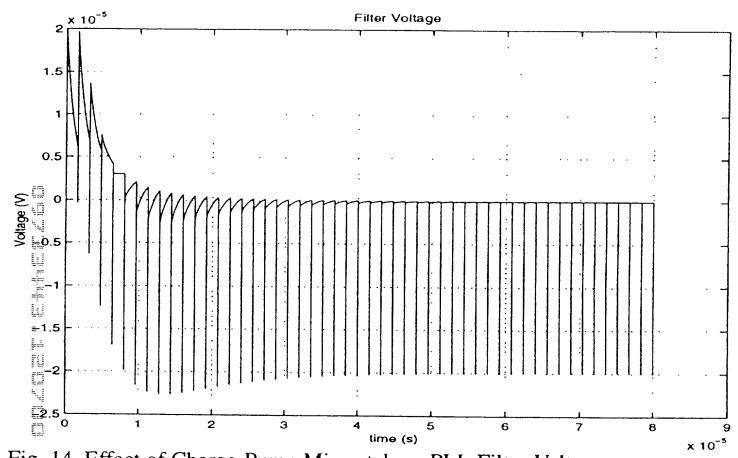


Fig. 14. Effect of Charge-Pump Mismatch on PLL Filter Voltage